## FIG 1

ASSIGN INTERRUPTS FOR I/O DEVICES
AMONG NODES OF NUMA SYSTEM, BASED
ON AT LEAST ONE OF: NODES TO WHICH I/O
DEVICES ARE CONNECTED, NODES AT
WHICH ISR'S FOR THE I/O DEVICES RESIDE,
AND PROCESSORS OF NODES
102

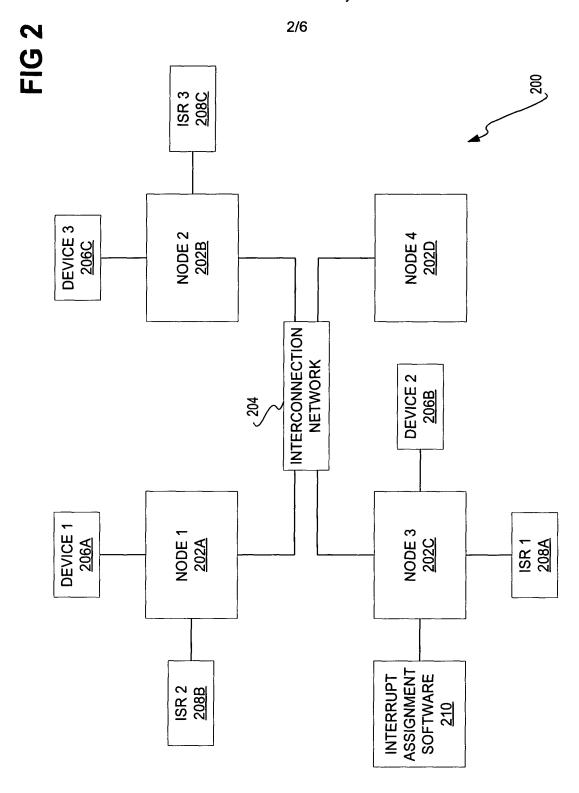
FOR EACH NUMA NODE, ASSIGN
INTERRUPTS FOR THE DEVICES THAT ARE
PERFORMANCE CRITICAL AND THAT HAVE
BEEN ASSIGNED TO THE NODE AMONG
PROCESSORS OF THE NODE IN ROUNDROBIN MANNER

104

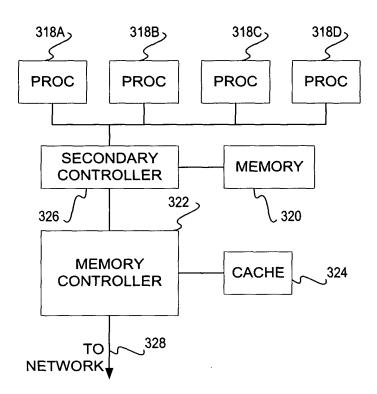
DYNAMICALLY MODIFY ASSIGNMENTS
OF INTERRUPTS AMONG NUMA NODES
BASED ON ACTUAL PERFORMANCE
CHARACTERISTICS OF THE
ASSIGNMENTS

<u>106</u>

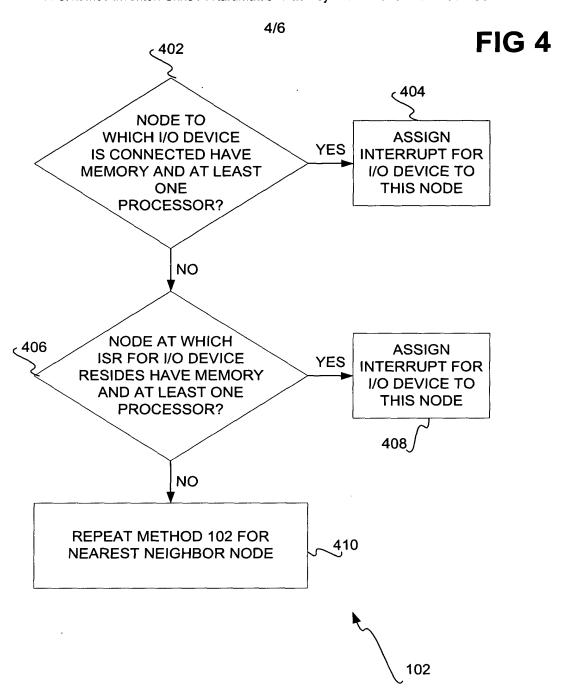
FOR EACH NUMA NODE, DYNAMICALLY MODIFY
ASSIGNMENTS OF INTERRUPTS THAT ARE
PERFORMANCE CRITICAL AND THAT HAVE BEEN
ASSIGNED TO THE NODE AMONG THE NODE'S
PROCESSORS BASED ON ACTUAL PERFORMANCE
CHARACTERISTICS OF THE ASSIGNMENTS
108

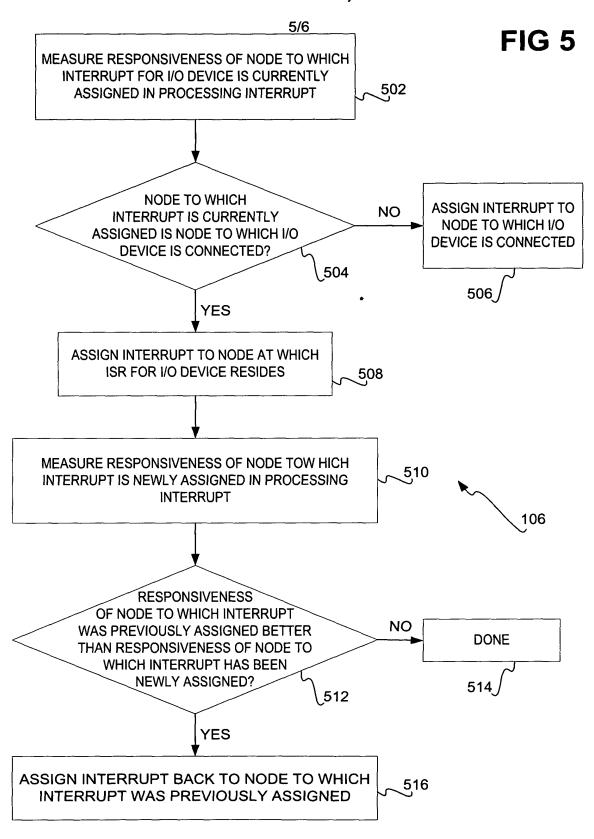


## FIG 3



## Assigning Interrupts For Input/Output (I/O) Devices Among Nodes Of A Non-Uniform Memory Access (Numa) System First named inventor: Chris P. Karamatas Attorney docket no. BEA920030013US1





<sup>6/6</sup> FIG 6

